International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622
National Level Technical Symposium On Emerging Trends in Engineering & Sciences
(NLTSETE&S- 13th & 14th March 2015)

RESEARCH ARTICLE OPEN ACCESS

Photo Voltaic Grid-Tied Inverters using H6 Transformer less Full-Bridge

N.SHIVTHEJ [1] , (M.TECH) ,G.ARUN SHEKAR[2], M.TECH.
Dept of Power Electronics and Electrical Drives, C.R.E.C, Tirupati, Andhra Pradesh, India[1]
Dept of Electrical & Electronics Engg, C.R.E.C, Tirupati, Andhra Pradesh, India[2]

Abstract
Photovoltaic (PV) generation systems are widely employed in transformer less inverters, in order to achieve the benefits of high efficiency and low cost. Safety requirements of leakage currents are met by proposing the various transformer less inverter topologies. In this paper, three transformer less inverter topologies are illustrated such as a family of H6 transformer less inverter topologies with low leakage currents is proposed, and the intrinsic relationship between H5 topology, highly efficient and reliable inverter concept (HERIC) topology. The proposed H6 topology has been discussed as well. For a detailed analysis with operation modes and modulation strategy one of the proposed H6 inverter topologies is taken as an example. Comparison among the HERIC, the H5, and the proposed H6 topologies is been done for the power device costs and power losses. For evaluating their performances in terms of power efficiency and leakage currents characteristics, a universal prototype is built for these three topologies mentioned. Experimental results show that the proposed HERIC topology and the H6 topology achieve similar performance in leakage currents, which is slightly worse than that of the H5 topology, but it features higher efficiency than that of H5 topology.

Index Terms: Grid-tied inverter, Common-mode voltage leak-age current, photovoltaic (PV) generation system, transformer less inverter**.**

I. INTRODUCTION

THE applications of distributed photovoltaic (PV) generation systems in both commercial and residential structures have rapidly increased during recent years. Although the price of PV panel has been declined largely, the overall cost of both the investment and generation of PV grid-tied system are still too high, comparing with other renewable energy sources. Therefore ,the grid-tied inverters need to be carefully designed for achieving the purposes of high efficiency, low cost, small size ,and low weight, especially in the low-power single-phase systems(less than 5 kW). From the safety point of view, most of

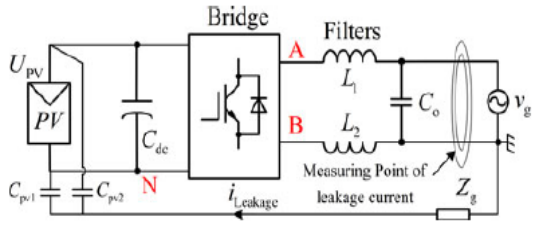


Fig. 1. Leakage current path for transformer less PV inverters.

the PV grid-tied inverters employ line-frequency transformers to provide galvanic isolation in commercial structures in the past. However, line-frequency transformers are large and heavy,making the whole system bulky and hard to install. Compared with line-frequency isolation, inverters with high-frequency isolationtransformers have lower cost, smaller size and weight.However, the inverters with high-frequency transformers haveseveral power stages, which increase the system complexityand reduce the system efficiency [1]–[6]. As a result, the transformerlessPV grid-tied inverters, as shown in Fig. 1, are widely installed in the low-power distributed PV generation systems .Unfortunately, when the transformer is removed, the common mode(CM) leakage currents (*I* leakage) may appear in the system and flow through the parasitic capacitances between the PV panels and the ground [7], [8]. Moreover, the leakage currents leadto serious safety and radiated interference issues [9]. Therefore ,they must be limited within a reasonable range [10].As shown in Fig. 1, the leakage current *I* Leakage is flowing through the loop consisting of the parasitic capacitances (*C*PV1and *C*PV2), bridge, filters (*L*1 and *L*2), utility grid, and ground impedance *Zg* . The leakage current path is equivalent to an *LC* resonant circuit in series with the CM voltage [11], and the CM voltage *v*CM is defined as

$V_{CM} = V_{AN} + V_{BN}\2+ (V_{AN} - V_{BN})(L2 - L1)\2(L1 + L2)$ (1)

where *v*AN is the voltage difference between points A and N,*v*BN is the voltage difference between points B and N. *L*1 and*L*2 are the output filter inductors .In order to eliminate leakage currents, the CM voltage mustbe kept constant or only varied at low frequency, such as50 Hz/60 Hz. The conventional solution employs the half-bridgeinverter [12], [13]. The filter inductor *L*2 is zero in the halfbridgeinverters. Therefore, (1) is simplified as

$$V_{CM} = V_{AN} + V_{BN}\2- (V_{AN} - V_{BN})\2= V_{BN}. \quad (2)$$

The CM voltage *v*CM is constant due to the neutral line ofthe utility grid connecting to the midpoint of the split dc-linkcapacitors directly.However, a drawback of half-bridge invertersis that, the dc voltage utilization of half-bridge type topologiesis half of the full-bridge topologies. As a resul t, either largenumbers of PV panels in series are nvolved or a boost dc/dcconverter with extremely high voltage transfer ratio is requiredas the first power conditioning stage, which could decrease thesystem efficiency.The full-bridge inverters only need half of the input voltagevalue demanded by the half-bridge topology, and the filter inductors*L*1 and *L*2 are usually with the same value. As a result,(1) is simplified as

$$V_{CM} = V_{AN} + V_{BN}\2 . \quad (3)$$

Many solutions have been proposed to realize CM voltage constantin the full-bridge transformerless inverters [14]–[25]. Atraditional method is to apply the full-bridge inverter with thebipolar sinusoidal pulsewidth modulation (SPWM). The CMvoltage of this inverter is kept constant during all operatingmodes. Thus, it features excellent leakage currents characteristic.However, the current ripples across the filter inductorsand the switching losses are likely to be large. The full-bridgeinverters with uniploar SPWM control are attractive due to theexcellent differential-mode (DM) characteristics such as smallerinductor current ripple, and higher conversion efficiency. However,the CM voltage of conventional unipolar SPWM fullbridgeinverter varies at switching frequency, which leads tohigh leakage currents [12]. However,these topologies have never been analyzed form the point of

view of topological relationships.In this paper, a family of novel H6 full-bridge topologies isproposed for the transformerless PV grid-tied inverters.An extra switch is inserted to the H5 topology for forming a new currentpath and for the purpose of reducing conduction loss. Therefore,in the active modes, the inductor current of the proposed H6topology flows through two switches during one of the halflineperiods and through three switches during another half-lineperiod. As a result, for comparing with the topologies presentedin [17], [19], and [20], the proposed H6 topology has achievedthe minimum conduction loss, and also has featured with lowleakage currents. On the other hand, the topological relationshipbetween H5 topology and HERIC topology is revealed, and themethods for generating HERIC topology from H6-type topology

and from hybrid-bridge topology are presented, respectively.This paper is organized as follows. In Section II, the operationmodes and characteristics of the H5 topology and theHERIC topologygenerating HERIC topology from the H6-type topology or fromthe hybrid-bridge topology are given. A family of H6 topologiesis proposed, and the topological relationship between H5topology and HERIC topology is analyzed. In Section III, oneof the proposed H6 topologies is taken as an example for analysisin detail with operational principle and modulation strategy.The comparisons between H5, HERIC, and the proposed H6topology are given in terms of power loss and device cost. Experimentalresults are presented in Section IV, and Section Vconcludes the paper.

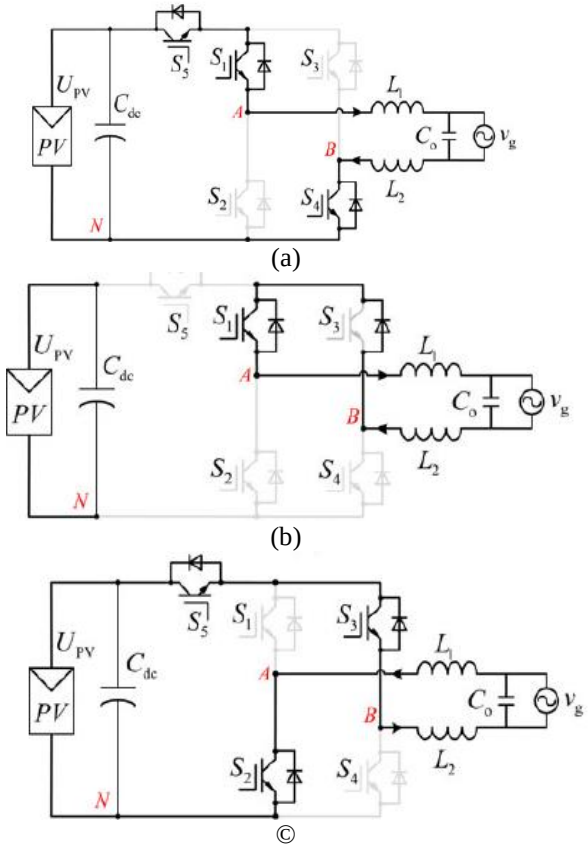
II. COMPARATIVE ANALYSIS ON EXISTING TOPOLOGIES

A. Operation Modes of H5 and HERIC

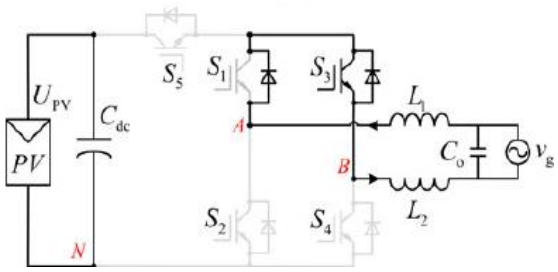
The operation modes of H5 topology and HERIC topologyare taken as examples for analysis. There are four operationmodes in each period of the utility grid of the H5 topology, asshown in Fig. 3. It can be seen that in the active modes, theinductor current of H5 topology is always flowing through threeswitches due to its extra switch *S*5 in dc side. In the freewheelingmodes, the inductor current of H5 topology is flowing throughtwo switches.There are four operation modes in each period of the utilitygrid of the HEIRC topology, as shown in Fig. 4. It can be seenthat the inductor current of HERIC topology is always flowingthrough two switches in the active modes. In the freewheelingmodes, the inductor current of HERIC topology is flowingthrough two switches.Therefore, although the H5 topology features less power devicesthan the HERIC topology, its conduction loss is highehigherthan that of the HERIC topology. Moreover, the conductionlosses of the H6-type topology and the hybrid-bridge topologyare also higher than that of the HERIC topology due to extraswitches in the dc side. As a result, the conduction losses of H5topology, H6-type topology, and hybrid-bridge topology shouldbe reduced for the harvest of higher efficiency.

B. Topology Relationship

The H6-type topology is taken as an example to analysisfirst. From Fig. 2(c), it can be seen that there are two switchesbetween the terminal (A) and the negative terminal of the PVarray, and there are another two switches between the terminal(B) and the negative terminal of the PV array. Therefore, theinductor current is controlled to flow through three switches inthe active modes of H6-type topology. In order to reduce theconduction loss, the collector of switch *S*2 is disconnected fromthe anode of diode *D*1 , and then it is connected to the terminal(A), as shown in Fig. 5(a). As a result, the inductor current flowsthrough *S*2 and S3 instead of *S*2, *S*3 , and *S*6 in the active modeduring the negative half cycle of the grid voltage. The dc and acsides of this topology are still disconnected in the freewheelingmodes. The same means are applied to another leg, where theswitch *S*4 is disconnected from the diode*D*2 and then connectedto the terminal (B), as shown in Fig. 5(b).Hence, a circuit structure of HERIC topology is derived by themethods described in Fig. 5. The topology is shown in Fig. 6



(a) (b) ©



(d)

.Fig. 3. Operation modes of H5 topology. (a) Active mode in the positive half period. (b) Freewheeling mode in the positive half period. (c) Active mode in the negative half period. (d) Freewheeling mode in the negative half period.

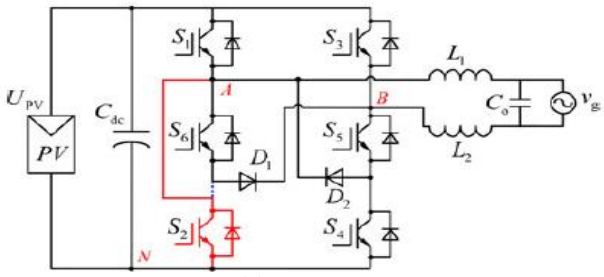
Compared with the HERIC topology shown in Fig. 2(c), the form of the bidirectional switch in ac side is changed.

Similarly, another circuit structure of HERIC topology can bederived from the hybrid-bridge shown in Fig. 2(d). The switches*S*3 and *S*4 are disconnected from *D*1 and *D*2 , respectively, andthen connect both of them to the terminal (B), as shown inFig. 7. However, there is only one extra switch in dc side of theH5 topology. When the emitter of *S*5 is disconnected from *S*1and connected to the terminal (A), the inductor current flowsthrough *S*4 and *S*5 instead of *S*1, *S*4 , and *S*5 in the active modeof positive half cycle of the grid voltage. Hence, the conductionloss is reduced. Unfortunately, in the active mode of negativehalf cycle of the grid voltage, there is no inductor current path, asshown in Fig. 8(a). Therefore, an extra switch *S*6 is introduced

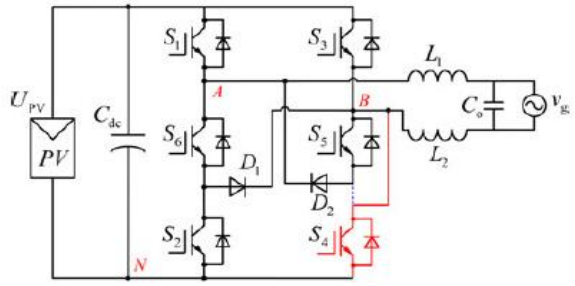
III. ANALYSIS ON THE H6 TOPOLOGY AND COMPARISONWITH OTHER TOPOLOGIES

A. Novel H6 Topology

From the aforementioned analysis, an extra switch *S*6 is introduced into the H5 inverter topology between the positive terminal of the PV array and the terminal (B) to form a new



(a)



(b)

Fig. 5. Modified H6-type inverter topologies. (a) Circuit structure A. (b) Circuit structure B.

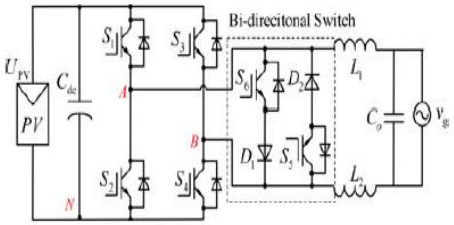


Fig. 6. Another circuit structure of HERIC topology.

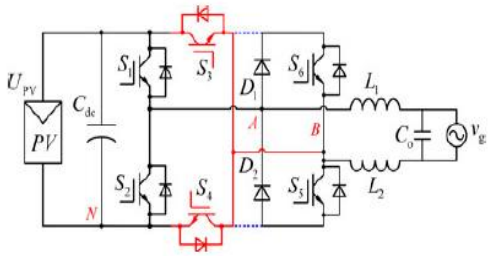
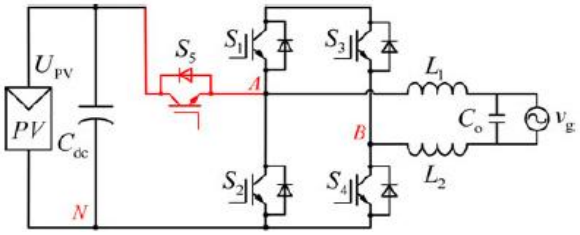
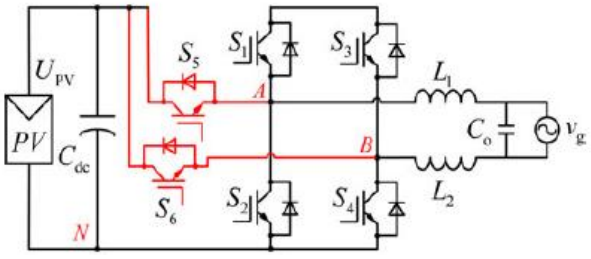


Fig. 7. Another circuit structure of HERIC topology derived from hybrid bridge topology .current path.

As a result, a novel H6 transformerless full-bridgeinverter topology is derived, as shown in Fig. 9(a).Similarly, the extra switch *S*6 can be introduced into the H5inverter topology between the positive terminal of the PV arrayand the terminal (A) to form a new current path as well, asshown in Fig. 9(b). Therefore, a new circuit structure of novelH6 inverter is presented. As a result, the conduction loss of theproposed H6 topologies is higher than HERIC topology and lessthan H5 topology.

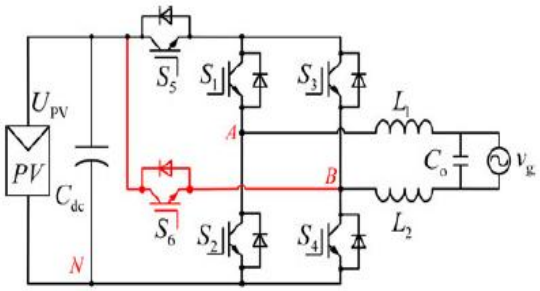


(a)



(b)

Fig. 8. Relationship between HERIC topology and H5 topology. (a) ModifiedH5 topology. (b) HERIC topology derived from H5 topology.



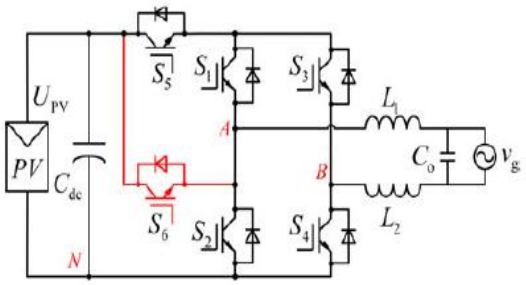


Fig. 9. A family of proposed H6-type inverter topologies. (a). Circuit structure A. (b) Circuit structure B.

B. Operation Mode Analysis

The circuit structure of proposed novel H6 inverter topologiesshown in Fig. 9(a) is taken as an example to analysis. PVgrid-tied systems usually operate with unity power factor. Thewaveforms of the gate drive signals for the proposed novel H6topology are shown in Fig. 10, where *vg* is the voltage of utilitygrid. *i*ref is the inductor current reference. *v*gs1 to *v*gs6 representthe gate drive signals of switches *S*1 to *S*6 , respectively.There are four operation modes in each period of the utilitygrid, as shown in Fig. 11, where *v*AN represents the voltagebetween terminal (A) and terminal (N) and *v*BN represents thevoltage between terminal (B) and terminal (N). *v*AB is the DM

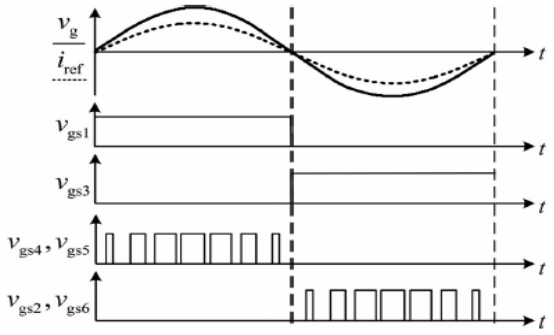


Fig. 10. Schematic of gate drive signals with unity power factor.

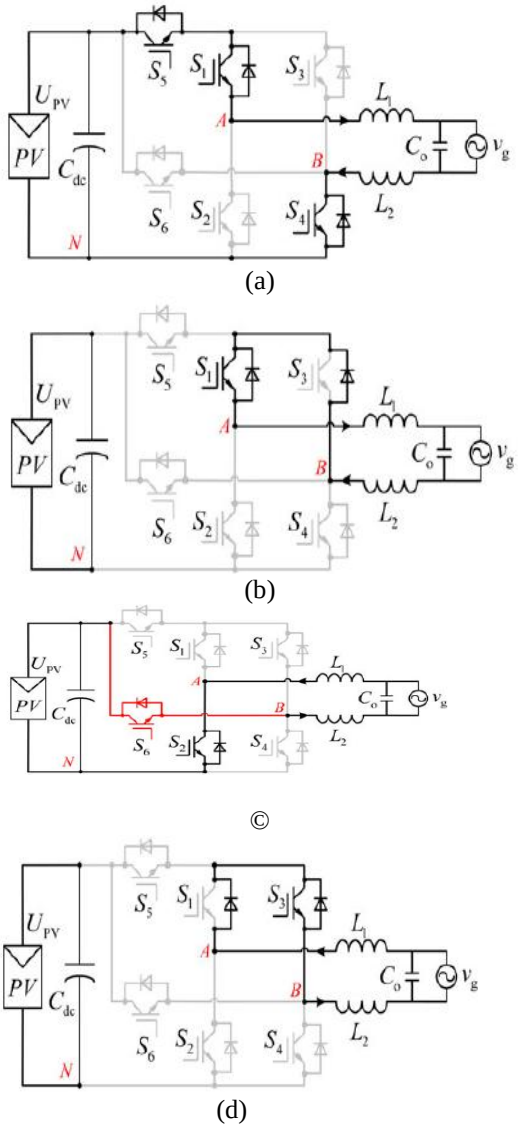


Fig. 11. Equivalent circuits of operation modes. (a)Active mode in the positive half period. (b) Freewheeling mode in the positive half period. (c) Active mode in the negative half period. (d) Freewheeling mode in the negative half period.

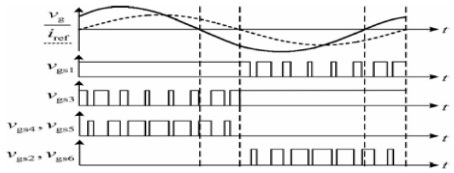


Fig. 12. Schematic of gate drive signals with power factor other than unity. voltage of the topology, *v*AB = *v*AN − *v*BN. The CM voltage*v*CM = 0.5(*v*AN + *v*BN).

a) Mode I is the active mode in the positive half period ofthe utility grid voltage, as shown in Fig. 11(a). *S*1, *S*4 ,and *S*5 are turned ON, and the other switches are turnedOFF. The inductor current is flowing through *S*1, *S*4 , and*S*5 . *v*AN = *U*PV, *v*BN = 0; thus, *v*AB = *U*PV, and the CMvoltage *v*CM = (*v*AN + *v*BN)/2 = 0.5*U*PV.b) Mode II is the freewheeling mode in the positive half periodof the utility grid voltage, as shown in Fig. 11(b). *S*1is turned ON; the other switches are turned OFF. The inductorcurrent is flowing through *S*1 and the antiparalleleddiode of *S*3 . *v*AN = *v*BN ≈ 0.5*U*PV; thus, *v*AB = 0, andthe CM voltage *v*CM = (*v*AN + *v*BN)/2 ≈ 0.5*U*PV.c) Mode III is the active mode in the negative half period ofthe utility grid voltage, as shown in Fig. 11(c). *S*2, *S*3 , and*S*6 are turned ON; the other switches are turned OFF. Theinductor current is flowing through *S*2 and *S*6 . Although*S*3 is turned ON, there is no current flowing through it, andthe switch *S*3 has no conduction loss in this mode. Nevertheless,in the H5 topology, the inductor current flowsthrough *S*2, *S*3 , and *S*5 . Therefore, the conduction loss ofproposed topology is less than that of H5 topology. In thismode, *v*AN = 0, *v*BN = *U*PV; thus, *v*AB = −*U*PV, and theCM voltage *v*CM = (*v*AN + *v*BN)/2 = 0.5*U*PV.d) Mode IV is the freewheeling mode in the negative half periodof the utility grid voltage, as shown in Fig. 11(d). *S*3is turned ON, and the other switches are turned OFF. Theinductor current is flowing through *S*3 and the antiparalleleddiode of *S*1 . *v*AN = *v*BN ≈ 0.5*U*PV; thus, *v*AB = 0,and the CM voltage *v*CM = (*v*AN + *v*BN)/2 ≈ 0.5*U*PV.Based on the aforementioned analysis, the PV array can bedisconnected from the utility grid when the output voltage ofthe proposed H6 inverter is at zero voltage level and the leakagecurrent path is cut off. The CMvoltage of the proposed topologyin each operation mode is equals to 0.5*U*PV, and it results in lowleakage current characteristic of the proposed H6 topologies.The proposed H6 topology with unipolar SPWM method notonly can achieve unity power factor, but also has the ability tocontrol the phase shifts between voltage and current waveforms.The modulation strategy is shown in Fig. 12. The drive signalis in phase with the grid-tied current. Therefore, it has the capa-

TABLE I
CALCULATED POWER LOSSES ON DEVICE

	S_1 (W)	S_2 (W)	S_3 (W)	S_4 (W)	S_5 (W)	S_6 (W)	Total losses(W)
H5	4.911	4.472	4.911	4.472	8.944	N.C.	27.71
HEIRC	4.472	4.472	4.472	4.472	2.571	2.571	23.03
H6	4.911	4.472	2.571	4.472	4.472	4.472	25.37

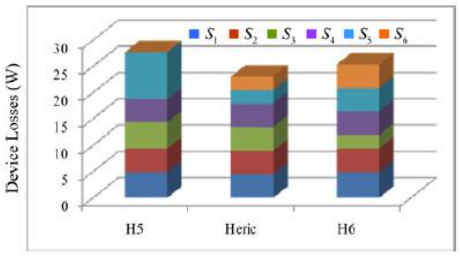


Fig. 13. Device losses distribution for these three topologies with 1 kW power rating.

TABLE II
COMPARISON OF OPERATING DEVICES IN THESE THREE TOPOLOGIES

		H5	HERIC	H6
Total device number		5	6	6
Isolated power supply for devices		4	3	4
Switching device number		2	2	2
Conducting device number	v_g>0	3	2	3
	v_g<0	3	2	2
Diodes number with freewheeling		2	2	2
Diodes number with reverse recovery		1	1	1
Gate drive number		2	2	2

TABLE III
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

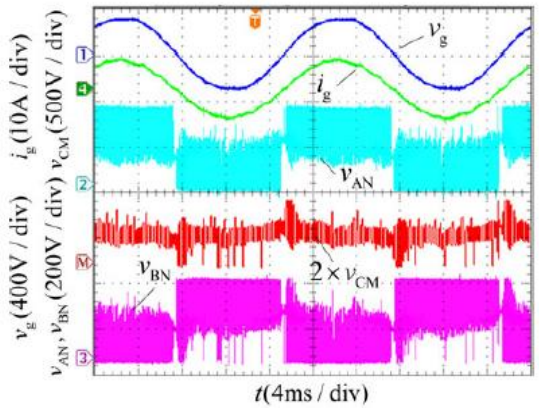
Parameter	Value
Rate power	1000 W
Input voltage	380~700 V
Grid voltage/frequency	230V/50Hz
Switching frequency	20kHz
Input Capacitance C_{dc}	940uF
Filter inductor L_1, L_2	3mH
Filter Capacitor C_o	0.47uF
Power Devices S_1~S_6 (IGBT)	IRG4PH40U
PV parasitic capacitances C_{PV1}, C_{PV2}	0.1uF

bility of injecting or absorbing reactive power, which meets thedemand for VDE-4105 standard.

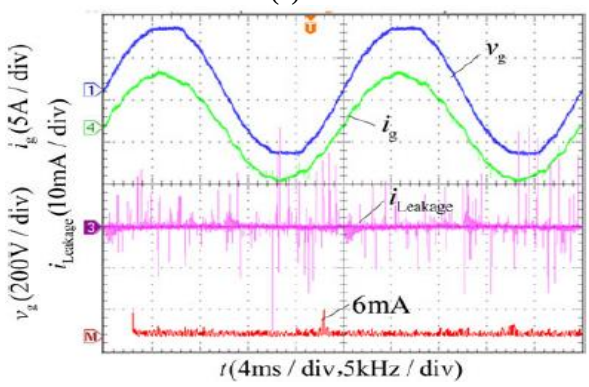
C. Comparisons of H5, HERIC, and the Proposed H6Topologies

The power losses of power switches of the proposed H6 topology[see Fig. 9(a)], H5 topology [see Fig. 2(a)], and HERICtopology [see Fig. 2(b)], are calculated with the same parametersas given in Table III, and are illustrated in Table I and Fig. 13.The calculationmethods and theories are studied and verified

Fig. 14. Picture of the universal prototype.



(a)



(b)

Fig. 15. CM voltage and leakage current in H5 topology. (a) CM voltage.(b) Leakage current.

in detail in literatures [22], [26]–[29], but not the contributionof this paper. On the other hand, the inductor losses in the threetopologies are the same due to the same *v*AB modulation. Therefore,the inductor losses of these three topologies are regardless.The comparison of operating devices in these three topologiesare summarized in Table II. The main power losses of switchesin each operation mode include the turn-ON/OFF loss, conduc-

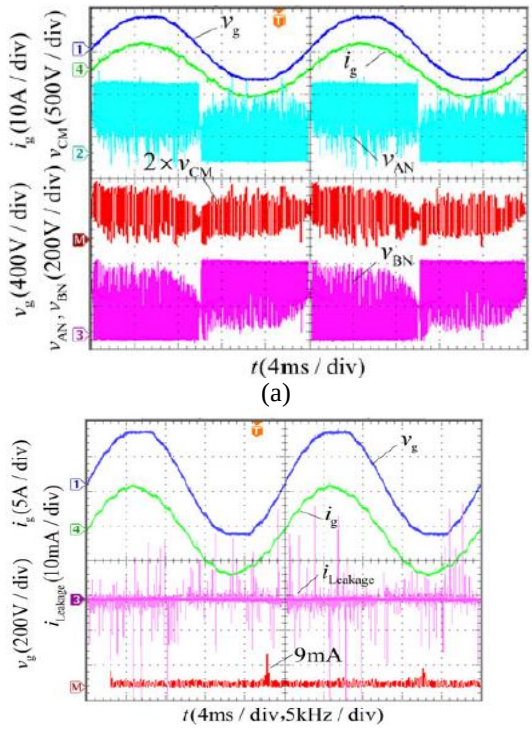


Fig. 16. CM voltage and leakage current in HERIC topology. (a) CM voltage.(b) Leakage current.

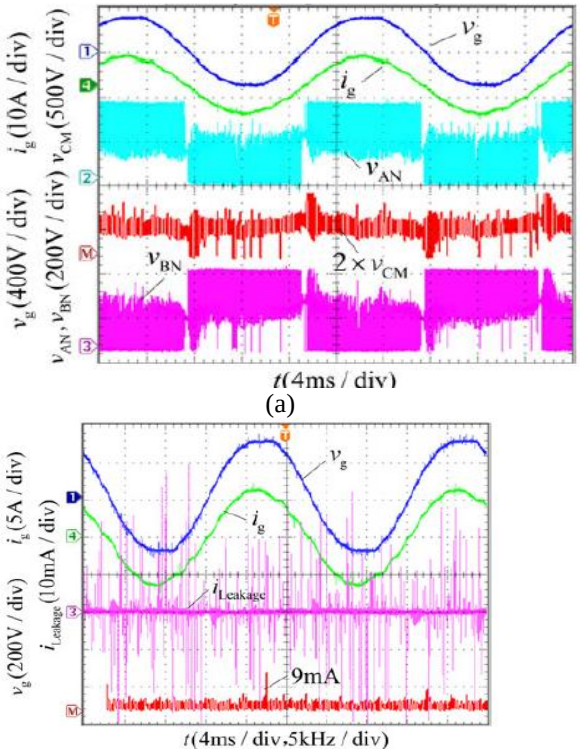


Fig. 17. CM voltage and leakage current in H6 topology. (a) CM voltage. (b) Leakage current.

tion loss, diode freewheeling loss, diode reverse recovery loss,and gate loss.From Tables I and II, it can be seen that the H5 topology onlyhas five power devices. Thus, it has the lowest device cost. Thedevice cost of HERIC and H6 is the same. The switching loss,diode freewheeling loss, diode reverse recovery loss, and gatedrive loss of these threetopologies are the same. However, H5topology has the highest conduction loss, and the conductionloss of the proposed H6 is higher than that of the HERIC topology.From Fig. 13, it can be seen that HERIC topology has the
best thermal stress distribution, while the H5 topology is theworst. The power loss of HERIC topology is the lowest.

IV. EXPERIMENTAL RESULTS

A universal prototype of H5 [see Fig. 2(a)], HERIC [seeFig. 2(b)], and novel H6 [see Fig. 9(a)] topologies has been builtup in order to verify the operation principle and compare theirperformances. The specifications of these three inverter topologiesare listed in Table III. The control circuit is implementedbased on a DSP chip TMS320F2808. The measure point ofleakage currents is shown in Fig. 1. Because *Zg* is very small, itis not being considered. The picture for the universal prototypeis depicted in Fig. 14. The YOKOGAWA WT1800 precision power analyzer was utilized as the measurement instrument tomeasure the efficiency of these three different topologies.The CM voltage and the leakage current waveforms of thesethree topologies in unified experimental conditions are shown inFigs. 15–17, respectively, where *vg* and *ig* are the grid voltageand grid-tied current, respectively. *v*AN and *v*BN are the voltagesbetween the midpoints A and B to terminal N, respectively. *v*CMis the CM voltage, which equals to 0.5(*v*AN + *v*BN). *i*leakagerepresents the leakage current.The leakage current measured for the H5, HERIC, and H6inverters at the switching frequency are 6 mA [see Fig. 15(b)], 9 mA [see Fig. 16(b)], and 9 mA [see Fig. 17(b)], respectively. The fast Fourier transform (FFT) results show that the leakagecurrent of H5 topology is the lowest, and the leakage current ofHERIC topology and H6 topology is almost the same.The drain–source voltage waveforms of switches in the novelH6 topology are shown in Fig. 18, where *v*ds5 and *v*ds6 aredrain–source voltages of *S*5 and *S*6 , respectively. From Fig. 18(b), it can be seen that in the negative half periodof the utility grid voltage, the voltage potential of the positiveterminal of the PV array is equal to that of the terminal (B),
so the drain–source voltage of switch *S*5 is zero. Thus, theswitch *S*5 only has switching loss in the positive half period

V. CONCLUSION

In this paper, from the topological relationship point of view,the intrinsic relationship between H5 topology and HERICtopology is revealed. The HERIC topology can be derived fromH5, H6-type, and hybrid-bridge topologies by the idea of reducingconduction loss. Moreover, based on the H5 topology, a newcurrent path is formed by inserting a power device between theterminals of PV array and the midpoint of one of bridge legs.As a result, a family of single-phase transformerless full-bridgeH6 inverter topologies with low leakage currents is derived.The proposed H6 topologies have the following advantages andevaluated by experimental results:

1) the conversion efficiency of the novel H6 topology is betterthan that of the H5 topology, and its thermal stress distribution is better than that of the H5 topology;
2) the leakage current is almost the same as HERIC topology,and meets the safety standard;
3) the excellentDMperformance is achieved like the isolatedfull-bridge inverter with uniploar SPWM. Therefore, the proposed H6 topologies are good solutions for the singlephasetransformerless PV grid-tied inverters.

REFERENCES

[1] S. B. Kjaer, J. K. Pederson, and F. Blaabjerg, "A review of single-phasegrid-connected inverters for photovoltaic modules," *IEEE Trans. Ind.Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep/Oct. 2005.

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficientinterface in dispersed power generation systems," *IEEE Trans. PowerElectron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[3] B. Sahan, A. N. Vergara, N. Henze, A. Engler, and P. Zacharias, "A singlestage PVmodule integrated converter based on a low-power current sourceinverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2602–2609, Jul. 2008.

[4] M. Calais, J. Myrzik, T. Spooner, and V. G. Agelidis, "Inverters for singlephase grid connected photovoltaic systems—An overview," in *Proc. IEEEPESC*, 2002, vol. 2, pp. 1995–2000.

[5] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficientinterface in dispersed power generation systems," *IEEE Trans. PowerElectron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[6] Q. Li and P. Wolfs, "A review of the single phase photovoltaic moduleintegrated converter topologies with three different dc link configuration,"*IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May2008.

[7] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesana, J.Malvar,R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in atransformerless photovoltaic application," *IEEE Trans. Energy Convers.*,vol. 25, no. 1, pp. 140–147, Mar. 2010.

[8] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, "Transformerlessinverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*,vol. 22, no. 2, pp. 693–697, Mar. 2007.

[9] H. Xiao and S. Xie, "Leakage current analytical model and applicationin single-phase transformerless photovoltaic grid-connected inverter,"*IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, Nov.2010.

N.SHIVTHEJ received B.Tech degree in Electrical & Electronics Engineering from KMMITS engineering college, Tirupati in 2012 and Presently pursuing M.Tech in Power Electronics and Drives from CREC, Tirupati, Andhra Pradesh, India.

G. ArunSekhar Received B. Tech Degree In Electrical & Electronics Engineering from ChadalawadaRamanamma Engineering College, Tirupati. M. Tech degree from Sri VenkatesaPerumal College of Engineering College, Puttur. Currently Working as Assistant Professor In the Department of Electrical & Electronics Engineering, Chadalawada Ramanamma Engineering College, Tirupati.